

WHAT WE CLAIM ARE:

- 1 . A semiconductor integrated circuit device comprising:
  - a semiconductor substrate defining a plurality of rows, each row including areas for a sequence of cells;
  - 5 a plurality of active regions disposed in each of said rows constituting semiconductor elements of associated cells;
  - a wiring region of stripe shape elongated along a direction of row, defined on said semiconductor substrate outside of said active regions in each row, and including wirings belonging to the associated cells, each wiring region having
  - 10 height in a direction crossing the row direction, the wiring region having locally different height.
- 2 . The semiconductor integrated circuit device according to claim 1, wherein said wiring regions of opposing cells in opposing rows have mutually fitting
- 15 shapes.
- 3 . The semiconductor integrated circuit device according to claim 1, wherein the wirings include a wiring made of a connection of different wiring layers.
- 20 4 . A method of manufacturing a semiconductor integrated circuit device comprising the steps of:
  - (a) decomposing circuit data into cells, and reading cell data including configuration data and interconnection data, from registered standard cell library;
  - (b) locating cells on a semiconductor substrate in a plurality of rows, each
  - 25 of said rows including a plurality of cells aligned along the direction of row, each

cell comprising active regions, shape-fixed wiring region disposed over the active region, and shape-variable wiring region disposed outside the active regions and having height along a direction crossing a direction of said row;

(c) designing layout of wirings in said shape-fixed wiring region;

5 (d) designing layout of wirings in said shape-variable wiring region;

(e) checking possible variation of wirings in said shape-variable wiring region which can reduce a distance between a pair of cells; and

(f) if there is a variation which can reduce the distance between said pair of cells, redesigning the layout of wirings in the shape-variable wiring region.

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5. The method of manufacturing a semiconductor integrated circuit device according to claim 4, further comprising the step of:

(g) repeating the steps of (e) and (f).

15 6. The method of manufacturing a semiconductor integrated circuit device according to claim 4, wherein said shape-variable wiring region in said step (b) has a rectangular shape of a fixed height, and the shape-variable wiring region in said steps (e) and (f) has locally variable height.

20 7. The method of manufacturing a semiconductor device according to claim 6, wherein said wirings are made of a plurality of wiring layers, and the shape-variable wiring region has locally variable height for each wiring layer.

8. The method of manufacturing a semiconductor integrated circuit device  
25 according to claim 4, wherein said step (e) checks density distribution of wirings

in said shape-variable wiring region.

9. The method of manufacturing a semiconductor integrated circuit device according to claim 4, wherein said step (f) changes the order of wirings in the  
5 direction of height.

10. The method of manufacturing a semiconductor integrated circuit device according to claim 9, wherein said step (f) includes changing at least part of a wiring with a different wiring layer.

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11. A method of automatically designing layout of a semiconductor integrated circuit device comprising the steps of:

(a) decomposing circuit data into cells, and reading cell data including configuration data and interconnection data, from registered standard cell library;

15 (b) locating cells on a semiconductor substrate in a plurality of rows, each of said rows including a plurality of cells aligned along direction of row, each cell comprising active regions, shape-fixed wiring region disposed over the active region, and shape-variable wiring region disposed outside the active regions and having height along a direction crossing the direction of row;

20 (c) designing layout of wirings in said shape-fixed wiring region;

(d) designing layout of wirings in said shape-variable wiring region;

(e) checking possible variation of wirings in said shape-variable wiring region which can reduce a distance between a pair of cells; and

(f) if there is a variation which can reduce the distance between said pair of  
25 cells, redesigning the layout of wirings in the shape-variable wiring region.

12. The method of automatically designing layout of a semiconductor integrated circuit device according to claim 11, further comprising the step of:

(g) repeating the steps of (e) and (f).

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13. The method of automatically designing layout of a semiconductor integrated circuit device according to claim 11, wherein said shape-variable wiring region in said step (b) has a rectangular shape of a fixed height, and the shape-variable wiring region in said steps (e) and (f) has locally variable height.

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14. The method of automatically designing layout of a semiconductor integrated circuit device according to claim 13, wherein said wirings are made of a plurality of wiring layers, and the shape-variable wiring region has locally variable height for each wiring layer.

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15. The method of automatically designing layout of a semiconductor integrated circuit device according to claim 11, wherein said step (e) checks density distribution of wirings in said shape-variable wiring region.

20 16. The method of automatically designing layout of a semiconductor integrated circuit device according to claim 11, wherein said step (f) changes the order of wirings in the direction of height.

17. The method of automatically designing layout of a semiconductor integrated  
25 circuit device according to claim 16, wherein said step (f) includes changing at

least part of a wiring with a different wiring layer.

18. A program for automatically designing layout of a semiconductor integrated circuit device, comprising the instructions of:

- 5        (a) decomposing circuit data into cells, and reading cell data including configuration data and interconnection data, from registered standard cell library;
- (b) locating cells on a semiconductor substrate in a plurality of rows, each of said rows including a plurality of cells aligned along direction of row, each cell comprising active regions, shape-fixed wiring region disposed over the active
- 10    region, and shape-variable wiring region disposed outside the active regions and having height along a direction crossing the direction of row;
- (c) designing layout of wirings in said shape-fixed wiring region;
- (d) designing layout of wirings in said shape-variable wiring region;
- (e) checking possible variation of wirings in said shape-variable wiring
- 15    region which can reduce a distance between a pair of cells; and
- (f) if there is a variation which can reduce the distance between said pair of cells, redesigning the layout of wirings in the shape-variable wiring region.